International Solid State Circuits Conference ISSCC 2002

Intel Corporation

Information under embargo until Monday, February 4, 2002

12:01 a.m. EST

Update on Intel Activities

- Pat Gelsinger, Intel Chief Technology Officer
- Justin Rattner, Intel Fellow and director of Microprocessor Research, Intel Labs
- Stefan Lai, vice president and co-director of Intel's California Technology and Manufacturing
- John Crawford, Intel Fellow and director of McKinley architecture

Last Year's ISSCC

- Gelsinger speech brought power as an issue to industry's attention
  - Biggest challenge moving forward is power delivery, dissipation and density
  - New challenges: Leakage, variations
  - "Performance at any cost" is history
  - Future is "balanced performance" – high performance, low power, low leakage

Intel at ISSCC 2002

- Eleven Intel papers in three areas:
- Circuit design
  - New techniques to enhance performance and lower both active and leakage power
- New details of next-generation Itanium™ processor (McKinley)
  - Low-latency Level 3 cache design for enhanced performance
- Next generation non-volatile memory (Ovonics)
  - New data from test chips

Circuit Design for High Performance and Low Power

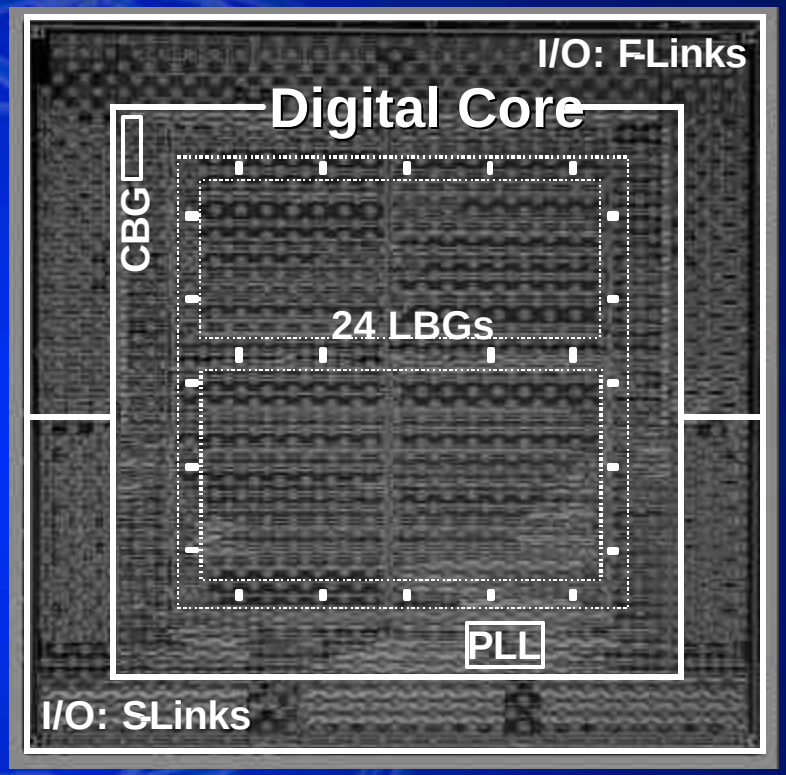
Justin Rattner

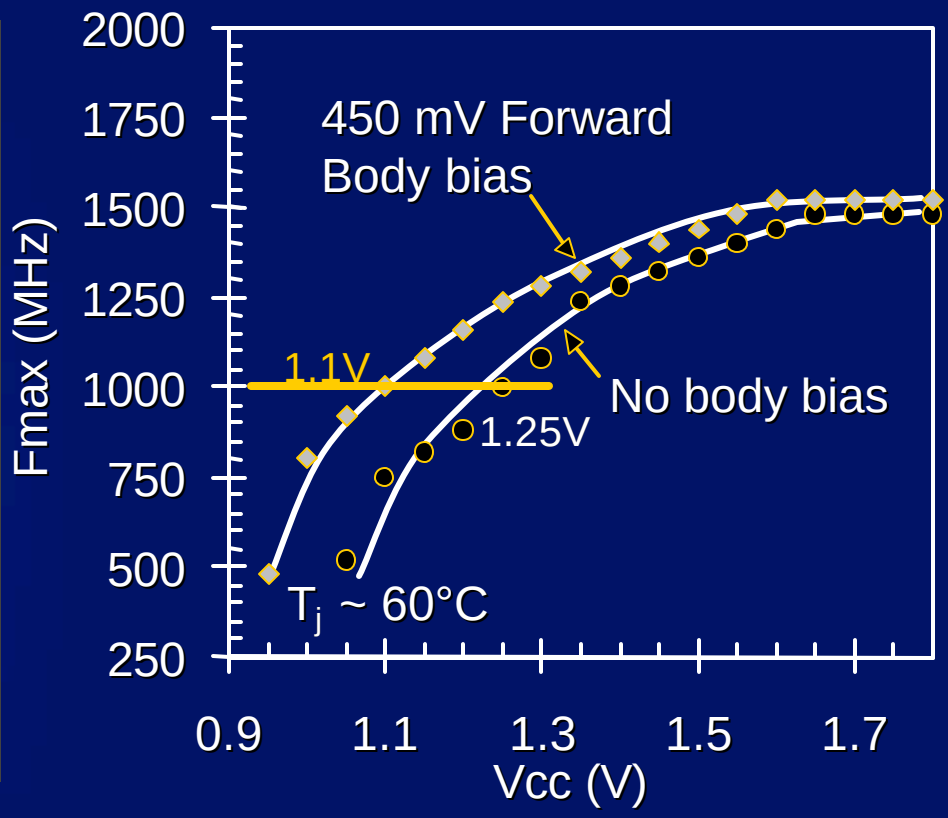
Intel Labs

Power Efficient Circuit Design

- Body bias
  - Benefits: Lowers active and leakage power
- Adaptive body bias
  - Benefits: Corrects power and improves yield
- Complementary signal generator
  - Benefit: Reduces die area and lowers power

Body Bias



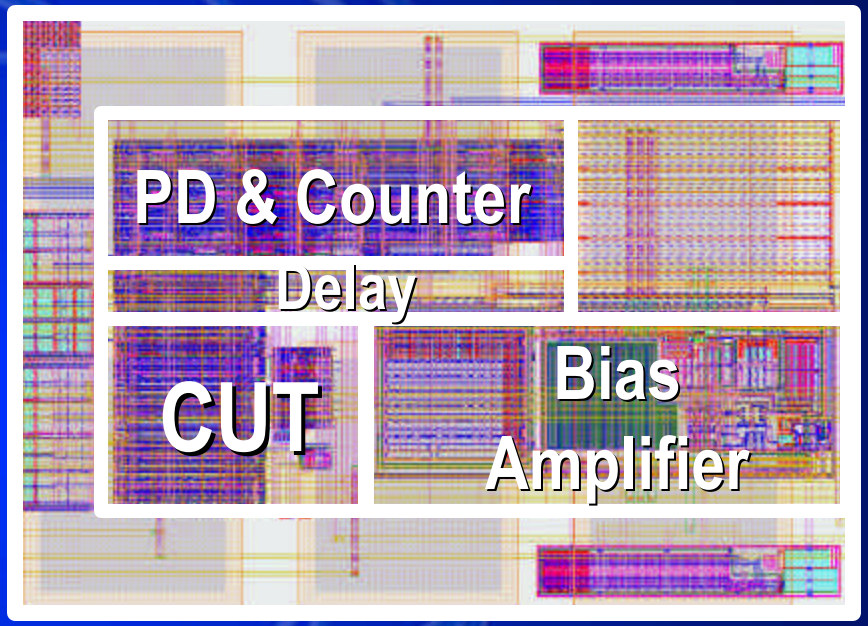


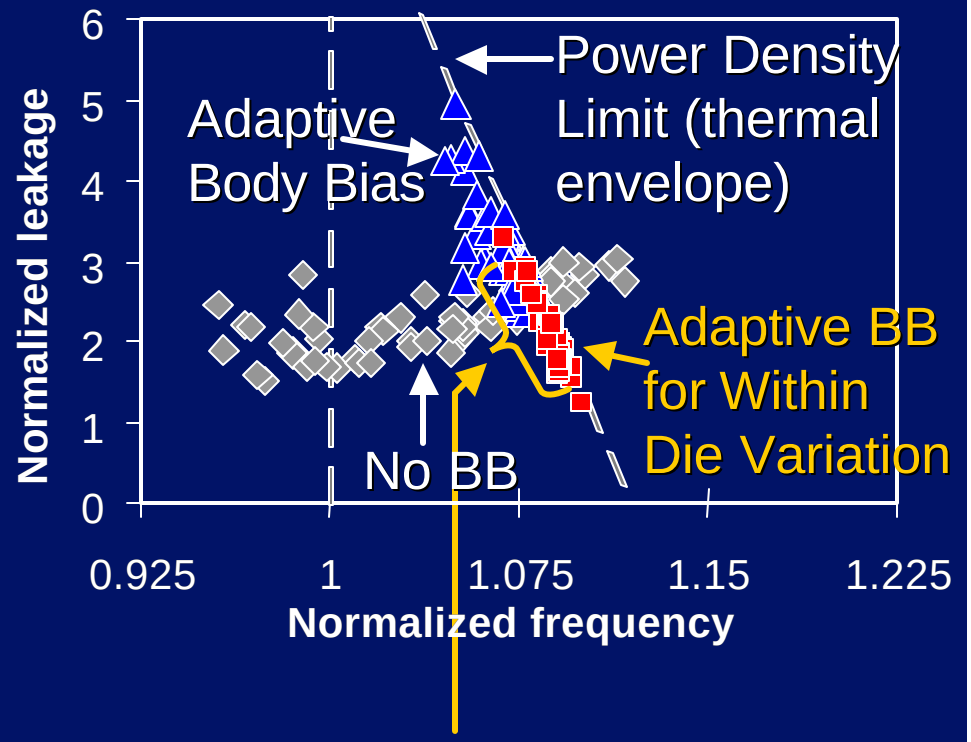
10.1 X 10.1 mm, 150nm CMOS
6.6 M Transistors, 1GHz

Paper 16.4:
1.1V 1GHz Communications Router with On-Chip Body Bias in 150nm CMOS

1. Forward bias enables 23% reduction in active power
2. Reverse bias cuts Stand-by leakage power 3.5X

Adaptive Body Bias





1.6 X 0.24 mm, 21 sites per die
150nm CMOS

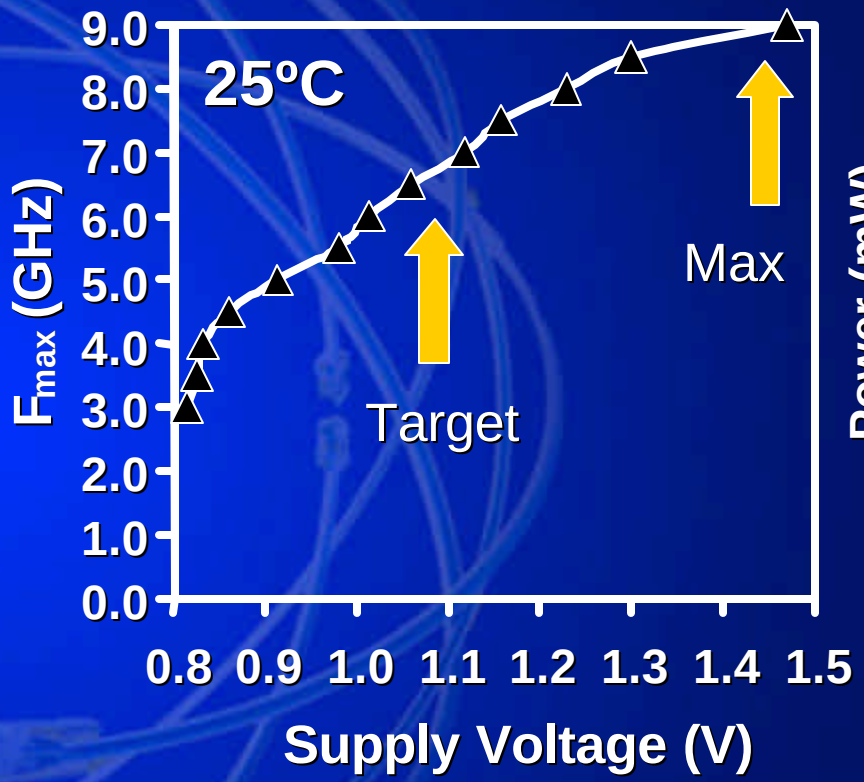
100 % Performance Yield
97% Highest Frequency Bin

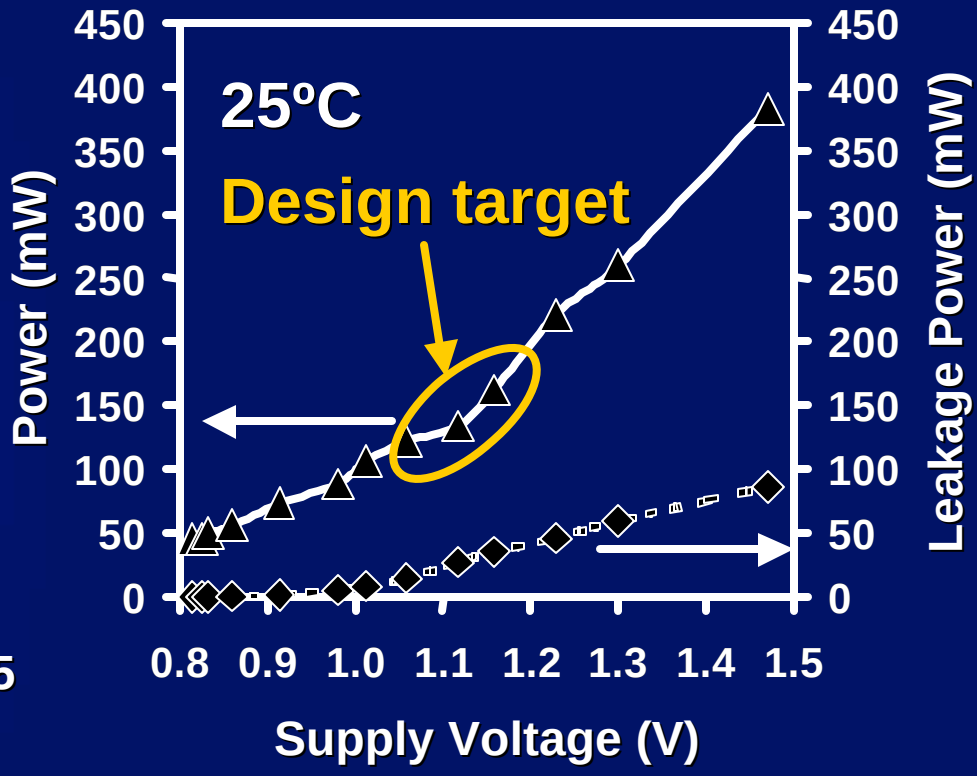
Paper 25.7: Adaptive Body Bias for Reducing Impacts of Die-to-Die and Within-Die Parameter Variations on Microprocessor Frequency and Leakage

Body Bias Techniques

- Applying body bias reduces active and leakage power
- Test chip demonstrate:
  - Active power reduced by 23 percent
  - Standby leakage reduced by 3.5 times
- Applying adaptive body bias produces more high frequency parts
- Test chip demonstrates:
  - 100 percent of die were high performance
  - 97 percent in the highest performance bin

6.5GHz ALU+Scheduler

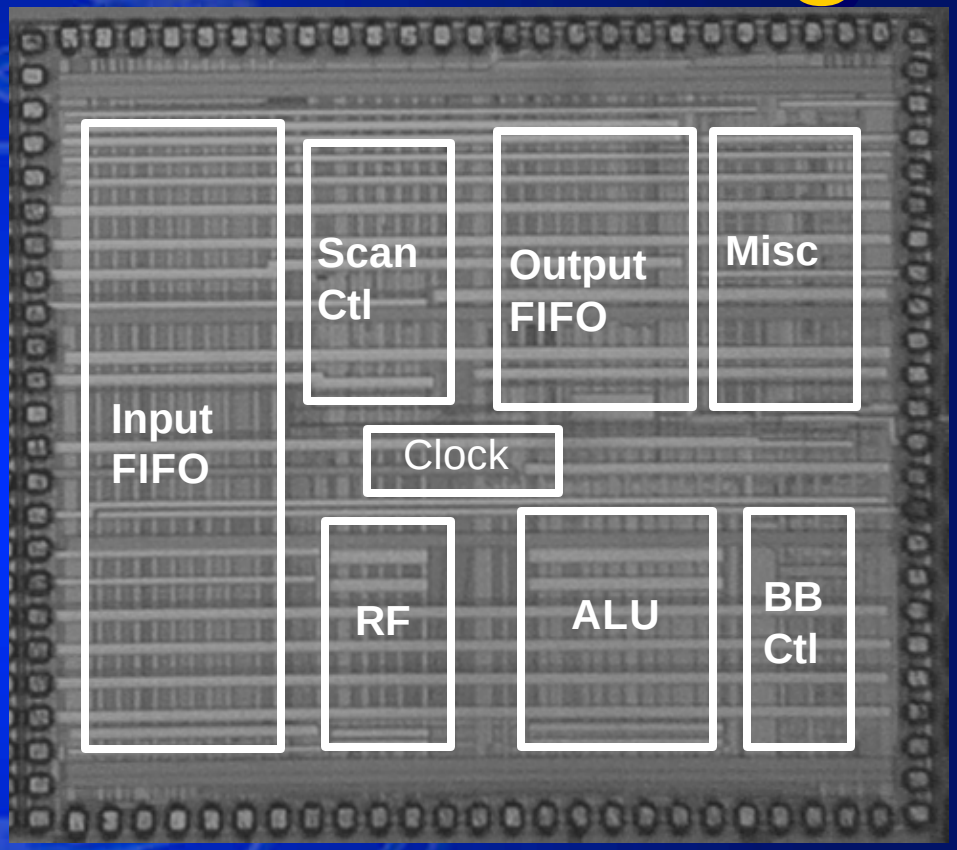


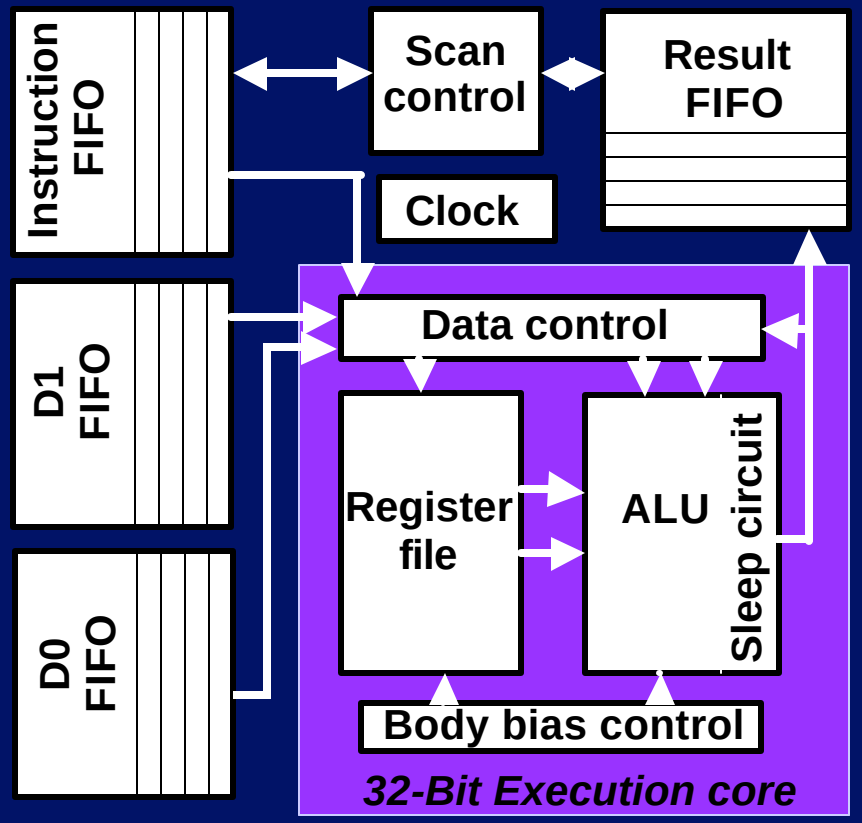


6.5GHz at 1.1V, 25ºC
Power: 120mW total, 15mW leakage
Scalable to 9GHz at 1.5V, 25ºC

Paper 25.1: A 6.5GHz 130nm Single-ended Dynamic ALU and Instruction Scheduler Loop

5 GHz Integer Exec Core





1.61 X 1.44 mm, 130nm Dual Vt CMOS
12 single clock cycle instructions
72 IO Pads, 267mW @5GHz, 30C

Paper 25.2: 5GHz, 32-Bit Integer Execution Core in 130nm Dual-V_T CMOS

Circuit technologies for high performance

1. Complementary signal generator
2. Stack node preconditioning
3. Leakage tolerance and reduction

Summary

Intel is responding to the power issue with high-performance, low-power circuits

- Applying body bias to reduce active and leakage power
- Applying adaptive body bias to improve yield
- Using CSG ALU to reduce circuit size
- Combining these technologies to demonstrate the first 5GHz microprocessor on 130nm technology at room temp

Update on Intel's Research on Ovonics Unified Memory

Stefan Lai

Intel Labs

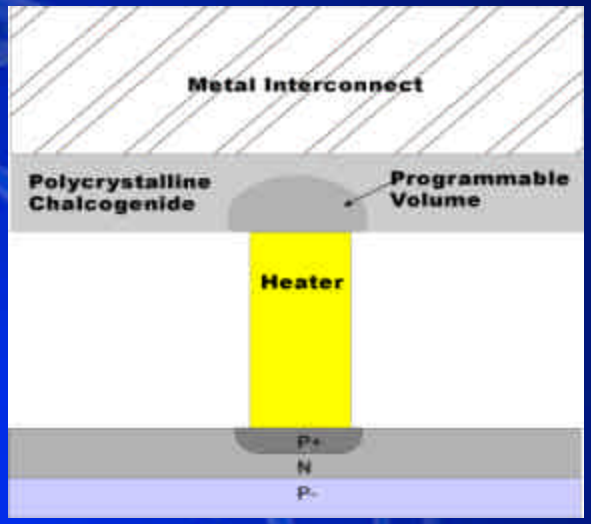
Next Generation Memory Research

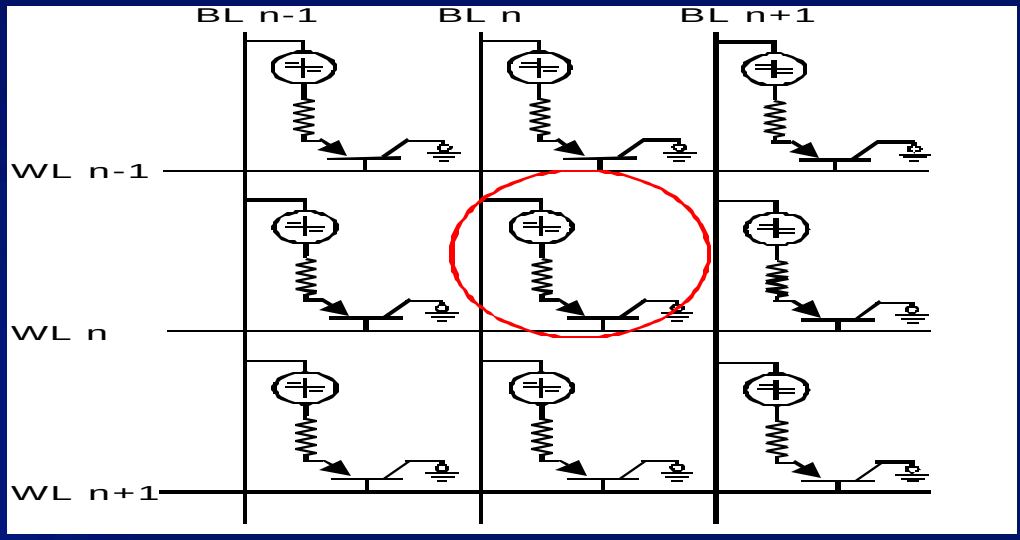
- Intel is conducting research on Ovonics Unified Memory for low cost, high performance non volatile memory
- In previous update (IEDM), reproducible switching elements have been reported
- In ISSCC, we are reporting data from a 4M array, showing capability of a high density memory

Array Architecture

- We have opted to use a diode as the switch in series with the ovonics switching element
  - Diode switch is easy to fabricate, is small and highly scalable and can carry high current required
  - Full array functionality has been demonstrated with good distribution and no array disturb

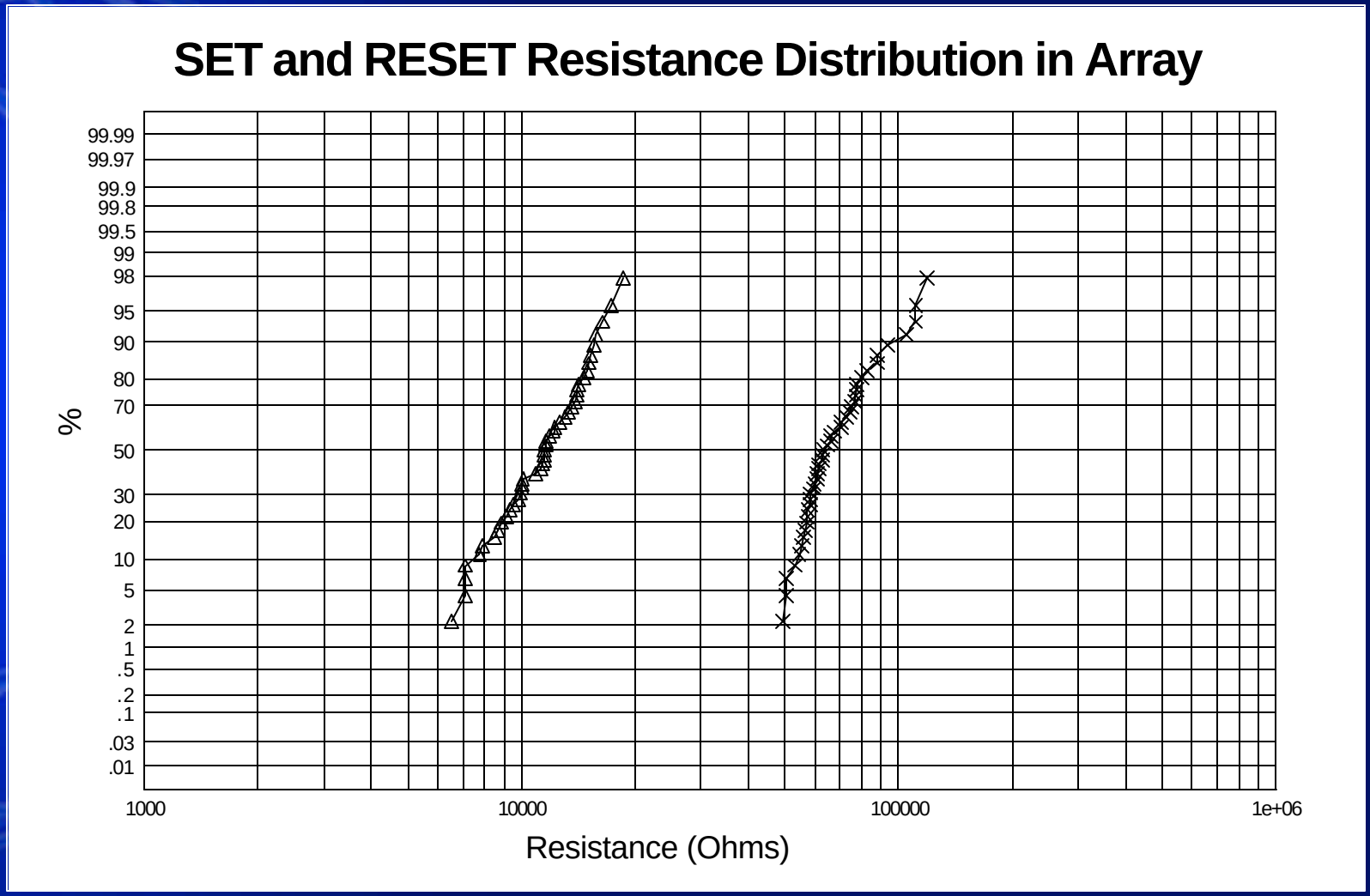
Memory Array Architecture





	Reset	Set	Read
BL n-1	0V	0V	0V
BL n	I_{reset}	I_{set}	I_{read}
BL n+1	0V	0V	0V
WL n-1	Vdd	Vdd	Vdd
WL n	0V	0V	0V
WL n+1	Vdd	Vdd	Vdd

Cell distribution data



Next Steps

- Current 0.18 ?m cell has too high program current (> 1 mA)
- Current 4M test chip allows detailed statistical study for cell and process improvement and will be near term focus
- Migrating development to 0.13 ?m process based on a new test vehicle design
- Data on new process and test vehicle 12 months from now

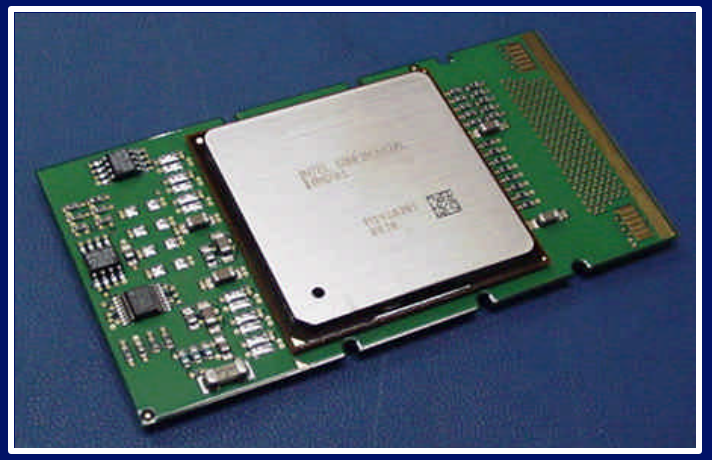
Update on Next-Generation Itanium™ Processor (McKinley)

John Crawford

Intel Labs

McKinley Update

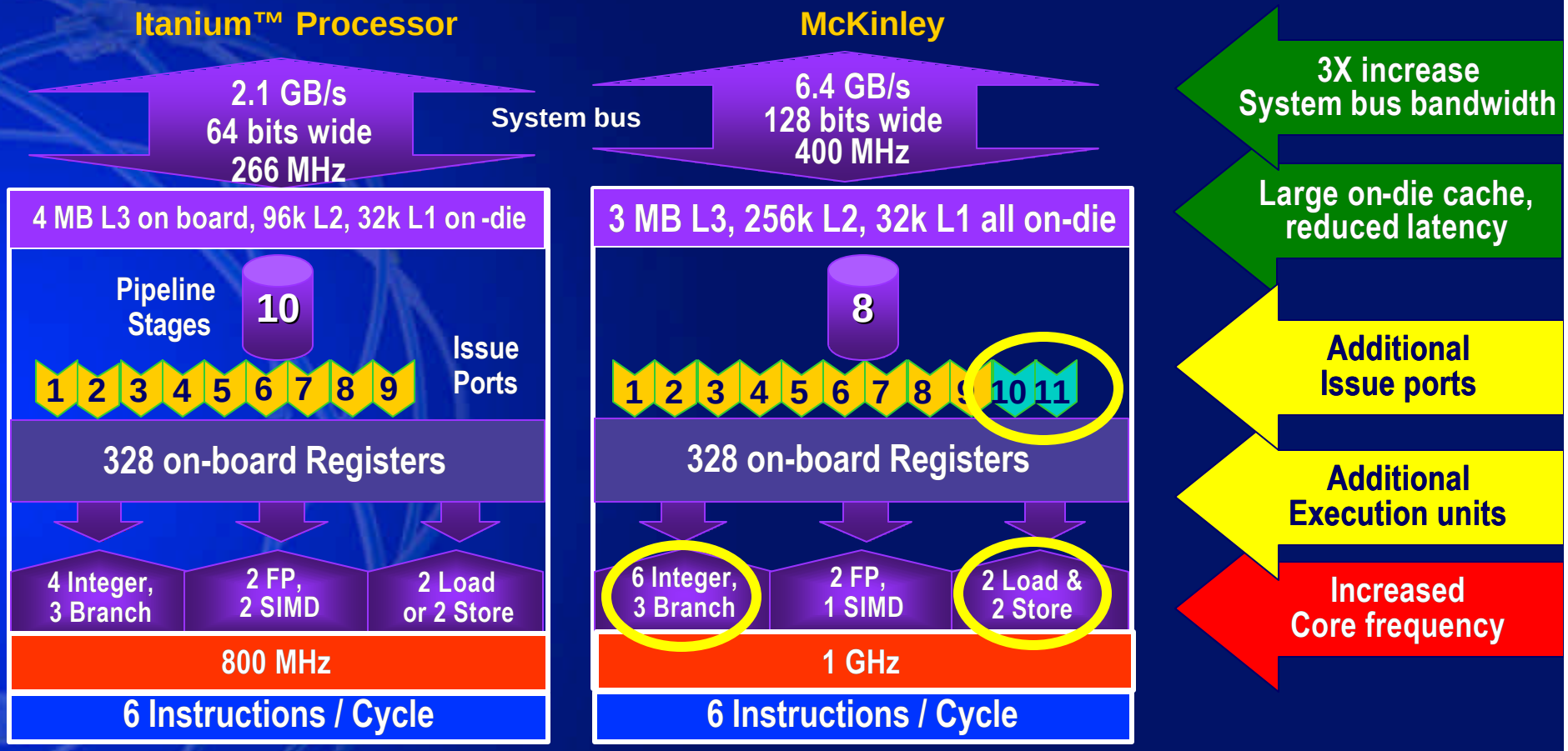
- McKinley on schedule for release in mid-2002
  - Sampling to OEMs since 02/01
  - Pre-production pilot systems underway with end users



- McKinley builds on and extends Itanium™ architecture
  - **Improved data speed and throughput**
  - **Additional execution resources for higher levels of parallelism**
  - **Compatible with Itanium-based software**

- **Estimate McKinley to deliver ~1.5-2X performance increase over Itanium-based systems**
- **Additional technical details disclosed at ISSCC '02**

Building Out the Itanium™ Architecture



McKinley delivers performance through:

- Bandwidth and cache improvements
- Micro-architecture enhancements
- Increased frequency

…and compatible with Itanium™ processor software

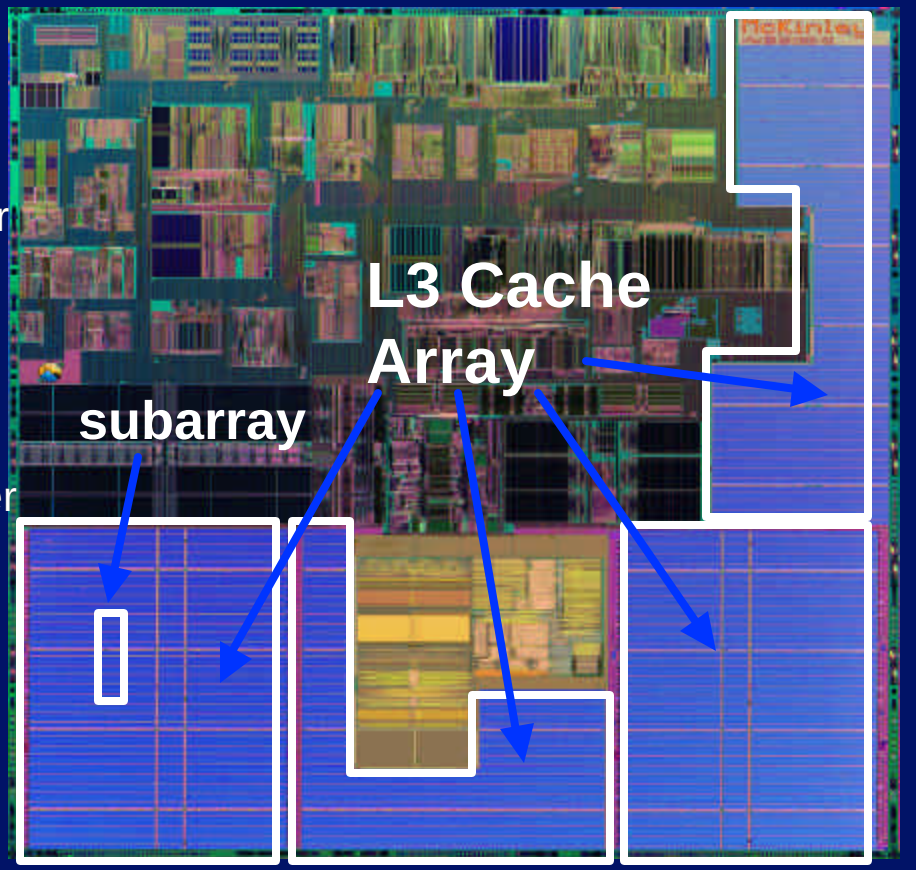
McKinley
221 million transistors total

McKinley at ISSCC

Intel and HP will co-present six papers on McKinley design at ISSCC

ISSCC Highlights

- Highly efficient design and layout of large on-die 3 MB L3 cache
  - McKinley cache is 85% efficient vs. ~70% for traditional cache designs
  - ~20% less area than traditional designs
  - Flexible to adjust to different floor plans
- Innovative L1 cache with 1-cycle latency
  - Enables ~15-25% performance increase over typical 2-3 cycle latency designs
  - No load delay penalties simplifies compiler scheduling
- 64 GB/s L2 cache bandwidth is up to 4X greater than proprietary RISC processors
- 6 issue integer execution units with full bypassing enables greater parallelism



McKinley Die

Summary

- McKinley is on schedule for mid-'02 platform release, and initial pilots have already begun
- Intel and HP will co-present six papers at ISSCC on McKinley's innovative cache and circuit design
- McKinley's unique design is expected to deliver ~1.5-2X performance over today's Itanium processor
- McKinley features:
  - Reduced cache latencies, including single-cycle L1 cache
  - 3MB of on-die cache
  - 3X increase in system bus bandwidth
  - 1GHz frequency
  - Additional execution units and issue ports

Backup

4M Test Chip Die Photo